**Amendments to the Drawings:**

The attached replacement sheet includes changes to Figure 2. This replacement sheet replaces the sheet that includes Figure 2. In Figure 2, the numeric labels 234 and 238 refer to elements that have the text "CPU". However, the Specification, as filed, describes numeric labels 234 and 238 as being CPU registers. (See page 14, line 11 through page 15, line 20 of the Specification, as filed). Herein, the text "CPU" has been removed to emphasize that numeric labels 234 and 238 refer to CPU registers instead of CPUs. No new matter was added.

Attachment: Replacement Sheet for Figure 2

## REMARKS

Claims 1-20 were previously pending in this patent application. Claims 1-20 stand rejected. Herein, Claims 1, 14, and 15 have been canceled. Claims 2-13 and 16-20 have been amended. Also, new Claims 21 and 22 have been added. Accordingly, after this Amendment and Response After Final Action, Claims 2-13 and 16-22 remain pending in this patent application. Further examination and reconsideration in view of the claims, remarks, and arguments set forth below is respectfully requested.

## SPECIFICATION

The specification has been amended to correct several typographical errors, to make clear that label 234 refers to a CPU register in Figure 2, and to make clear that label 238 refers to a CPU register in Figure 2. No new matter was added.

## DRAWINGS

In Figure 2, the text "CPU" has been removed to emphasize that numeric labels 234 and 238 refer to CPU registers instead of CPUs. No new matter was added.

## 35 U.S.C. Section 112, First Paragraph and Second Paragraph Rejections

Claims 7, 8, and 19 stand rejected under 35 U.S.C. Section 112, First Paragraph and Second Paragraph. The amendments to Claims 7, 8, and 19 render these rejections moot.

35 U.S.C. Section 103(a) Rejections

Claims 1-2, 5-11, 13-16, and 18-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al., U.S. Patent No. 5,357,626 (hereafter Johnson), in view of Grunert, U.S. Patent No. 6,366,878 (hereafter Grunert), and further in view of Jackson, U.S. Patent No. 4,176,258 (hereafter Jackson). These rejections are respectfully traversed. Since Claims 1, 14, and 15 have been canceled, the rejections against Claims 1, 14, and 15 are now moot. Dependent Claims 2 and 5-8 now depend from new Independent Claim 21. Similarly, Dependent Claims 16 and 18-20 now depend from new Independent Claim 22.

Independent Claim 21 recites:

> "A system for debugging microcontroller code, comprising:
> a target microcontroller including a first memory;
> an in circuit emulator base station including a second memory and an emulated target microcontroller which is not identical to and emulates operation of said target microcontroller, wherein said target microcontroller and said emulated target microcontroller execute said microcontroller code, wherein said microcontroller code execution occurs in lock step by executing same instructions using same clocking signals; and
> an interface coupled to said target microcontroller and said in circuit emulator base station, wherein lock step of said microcontroller code execution is verified by comparing said first memory with said second memory solely on occurrence of any one of said microcontroller code execution encounters a breakpoint and said microcontroller code execution halts, and wherein a mismatch between said first and second memories initiates debugging said microcontroller code." (emphasis added)

To establish a *prima facie* case of obviousness pursuant to 35 U.S.C. 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally

available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure.

It is respectfully asserted that there is no teaching, suggestion, or motivation to modify or combine Johnson, Grunert, and Jackson and that there is no reasonable expectation of success if Johnson, Grunert, and Jackson are modified or combined. More importantly, the modified or combined references Johnson, Grunert, and Jackson fail to teach, suggest, or motivate all the claim limitations of Independent Claim 21.

Independent Claim 21 recites the claim limitations, "a target microcontroller," and, "an emulated target microcontroller which is not identical to and emulates operation of said target microcontroller," (emphasis added). On page 13 of the Final Office Action, the passage, "To enable the second processor 14 to duplicate the executions of the first processor 12," at Col. 4, lines 31-34, of Johnson is cited to establish that the second processor 14 emulates the first processor 12 in Figure 1 of Johnson. However, Johnson states, "each of the processors 12 and 14 is preferably an AM29030/35 microprocessor." (Johnson, Col. 9, lines 9-11). That is, the second processor 14 and the first processor 12 are identical. In contrast, Independent Claim 21 is directed to an emulated target microcontroller which is not identical to and emulates operation of the target microcontroller and is directed to microcontrollers instead of processors.

Continuing, the Final Office Action admits, at page 13, that Johnson does not expressly teach that the processors are microcontrollers. The Final Office Action, at page 13, goes on to cite Grunert as teaching use of microcontrollers and as teaching the second microcontroller emulates the first microcontroller. However, Grunert states, "the invention, for in circuit emulation comprises two identical microcontrollers," (emphasis added) at Col. 1, lines 48-49, "first and second identical microcontrollers (2, 3)," (emphasis added) at Col. 2, line 1, and "two microcontrollers 2, 3 of identical design," (emphasis added) at Col. 4, lines 27-28. This is clearly distinguishable from Independent Claim 21, which is directed to an emulated target microcontroller which is not identical to and emulates operation of the target microcontroller.

Further, Independent Claim 21 recites the claim limitation, "wherein lock step of said microcontroller code execution is verified by comparing said first memory with said second memory solely on occurrence of any one of said microcontroller code execution encounters a breakpoint and said microcontroller code execution halts," (emphasis added). It is admitted at page 14 of the Final Office Action that Johnson in view of Grunert does not expressly teach comparing contents of a first memory against contents of the second memory to verify the lock step operation. However, on pages 14-15 of the Final Office Action, Jackson is cited as teaching comparing contents of a first memory against contents of a second memory to verify lock step. Also, on pages 10 and 18 of the Final Office Action, it is stated, "the Jackson reference teaches verifying lockstep continuously," (emphasis in quotation). Similarly, on page 18 of the Final Office Action, it is stated, "Jackson teaches 'comparing' at all times, including when the execution of code is halted," (emphasis added). Unlike

Jackson, Independent Claim 21 is directed to verifying lock step solely on occurrence of any one of the microcontroller code execution encounters a breakpoint and the microcontroller code execution halts instead of being directed to verifying lockstep continuously.

As discussed in detail above, the modified or combined references Johnson, Grunert, and Jackson fail to teach, suggest, or motivate all the claim limitations of Independent Claim 21. Therefore, it is respectfully submitted that Independent Claim 21 is patentable over the modified or combined references Johnson, Grunert, and Jackson and is in condition for allowance.

Dependent Claims 2 and 5-8 are dependent on allowable Independent Claim 21, which is allowable over the modified or combined references Johnson, Grunert, and Jackson. Hence, it is respectfully submitted that Dependent Claims 2 and 5-8 are patentable over the modified or combined references Johnson, Grunert, and Jackson for the reasons discussed above.

With respect to Independent Claims 9 and 22, it is respectfully submitted that Independent Claims 9 and 22 recite similar limitations as in Independent Claim 21. In particular, Independent Claim 9 recites the limitations, "programming said microcontroller code into a target microcontroller including a first memory and into an in circuit emulator base station including a second memory, a trace buffer, and an emulated target microcontroller which is not identical to and emulates operation of said target microcontroller," (emphasis added), and, "verifying lock step of said executing step by comparing content of the first memory and content of the second memory solely on occurrence of any one of said executing step encounters a breakpoint and said executing step

halts," (emphasis added). Independent Claim 22 recites the limitations, "an emulated target microcontroller which is not identical to and emulates operation of said target microcontroller," (emphasis added), and, "wherein lock step of said microcontroller code execution is verified by said computer system by comparing said first memory with said second memory solely on occurrence of any one of said microcontroller code execution encounters a breakpoint and said microcontroller code execution halts," (emphasis added).

The modified or combined references Johnson, Grunert, and Jackson fail to teach, suggest, or motivate all the claim limitations of Independent Claims 9 and 22, including the cited claim limitations for the reasons noted above. Therefore, Independent Claims 9 and 22 are patentable over the modified or combined references Johnson, Grunert, and Jackson and are in condition for allowance for reasons discussed in connection with Independent Claim 21.

Dependent Claims 10-11 and 13 and Dependent Claims 16 and 18-20 are dependent on allowable Independent Claims 9 and 22, respectively, which are allowable over the modified or combined references Johnson, Grunert, and Jackson. Hence, it is respectfully submitted that Dependent Claims 10-11 and 13, and Dependent Claims 16 and 18-20 are patentable over the modified or combined references Johnson, Grunert, and Jackson for the reasons discussed above.

Claims 3, 12, and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al., U.S. Patent No. 5,357,626 (hereafter Johnson), in view of Grunert, U.S. Patent No. 6,366,878 (hereafter Grunert), in

view of Jackson, U.S. Patent No. 4,176,258 (hereafter Jackson), and further in view of Barnett, U.S. Patent No. 6,173,419 (hereafter Barnett). These rejections are respectfully traversed. Dependent Claim 3 now depends from new Independent Claim 21. Similarly, Dependent Claim 17 now depends from new Independent Claim 22.

Since Independent Claims 21, 9, and 22 are patentable over the modified or combined references Johnson, Grunert, and Jackson, the respective Dependent Claims 3, 12, and 17 are patentable over the modified or combined references Johnson, Grunert, and Jackson for the reasons discussed above. Dependent Claims 3, 12, and 17 recite the claim limitation, "said in circuit emulator base station includes a field programmable gate array (FPGA), and wherein said emulated target microcontroller is programmed into said FPGA." On page 20 of the Final Office Action, it is admitted that none of Johnson, Grunert, or Jackson expressly teaches a relationship between a microcontroller and an FPGA. The Final Office Action, at page 20, goes on to cite the reference Barnett as teaching an FPGA programmed to emulate a microcontroller.

However, Barnett fails to remedy the deficiencies of the modified or combined references Johnson, Grunert, and Jackson discussed above. Moreover, Barnett teaches away from employing its teachings in the inventions represented by Dependent Claim 3 (which incorporates the claim limitations of Independent Claim 21), Dependent Claim 12 (which incorporates the claim limitations of Independent Claim 9), and Dependent Claim 17 (which incorporates the claim limitations of Independent Claim 22). In particular, Barnett states, "In contrast, the emulator programmed into the FPGA is identical to the target CPU IC logic but not in timing since the two are in different forms of

silicon. The FPGA is not able to handle the timing and asynchronous signals of the signals on the pins of a target CPU," (emphasis added) at Col. 6, line 64 through Col. 7, line 2. A person of ordinary skill in the art at the time of Applicant's invention would be discouraged to use the teachings of Barnett because in Dependent Claim 3 (which incorporates the claim limitations of Independent Claim 21), Dependent Claim 12 (which incorporates the claim limitations of Independent Claim 9), and Dependent Claim 17 (which incorporates the claim limitations of Independent Claim 22) microcontroller code execution (by target microcontroller and emulated target microcontroller that is programmed into the FPGA) occurs in lock step by executing same instructions using same clocking signals.

Further, Barnett shows in Figure 6 that the FPGA 100 programmed with the emulated target CPU 102 takes the place of the target CPU in the debugging apparatus. Also, Barnett states, "The second type of software debugging tool is an emulator that substitutes for the target micro-controller during target circuit testing and execution," (emphasis added), at Col. 1, lines 39-42. A person of ordinary skill in the art at the time of Applicant's invention would be discouraged to use the teachings of Barnett because in Dependent Claim 3 (which incorporates the claim limitations of Independent Claim 21), Dependent Claim 12 (which incorporates the claim limitations of Independent Claim 9), and Dependent Claim 17 (which incorporates the claim limitations of Independent Claim 22) a target microcontroller and an emulated target microcontroller that is programmed into the FPGA are utilized in a debugging apparatus instead of utilizing solely the emulated target microcontroller that is programmed into the FPGA.

As discussed in detail above, the modified or combined references Johnson, Grunert, Jackson, and Barnet fail to teach, suggest, or motivate all the claim limitations of Dependent Claims 3, 12, and 17. Therefore, it is respectfully submitted that Dependent Claims 3, 12, and 17 are patentable over the modified or combined references Johnson, Grunert, Jackson, and Barnet and are in condition for allowance.

Claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al., U.S. Patent No. 5,357,626 (hereafter Johnson), in view of Grunert, U.S. Patent No. 6,366,878 (hereafter Grunert), in view of Jackson, U.S. Patent No. 4,176,258 (hereafter Jackson), and further in view of "State of the Art" by Stan Augarten, published 1983 (hereafter Augarten). This rejection is respectfully traversed. Dependent Claim 4 now depends from new Independent Claim 21.

Since Independent Claim 21 is patentable over the modified or combined references Johnson, Grunert, and Jackson, the respective Dependent Claim 4 is patentable over the modified or combined references Johnson, Grunert, and Jackson for the reasons discussed above. Dependent Claim 4 recites the claim limitation, "the first memory includes a first static random access memory (SRAM) and the second memory includes a second SRAM." On page 21 of the Final Office Action, it is admitted that none of Johnson, Grunert, or Jackson expressly teaches that the first and second memories are SRAM. The Final Office Action, at page 21, goes on to cite the reference Augarten as disclosing SRAM and its advantages.

However, Augarten fails to remedy the deficiencies of the modified or combined references Johnson, Grunert, and Jackson discussed above. Thus, the modified or combined references Johnson, Grunert, Jackson, and Augarten fail to teach, suggest, or motivate all the claim limitations of Dependent Claim 4. Therefore, it is respectfully submitted that Dependent Claim 4 is patentable over the modified or combined references Johnson, Grunert, Jackson, and Augarten and is in condition for allowance.

## CONCLUSION

It is respectfully submitted that the above claims, arguments and remarks overcome all rejections and objections. All remaining claims (Claims 2-13 and 16-22) are neither anticipated nor obvious in view of the cited references. For at least the above-presented reasons, it is respectfully submitted that all remaining claims (Claims 2-13 and 16-22) are in condition for allowance.

The Examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

MURABITO HAO & BARNES, LLP

Dated: 4/12/2007

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Attachment: One Replacement Sheet